

Notice of References CitedApplication/Control No.
09/776,387Applicant(s)/Patent Under
Reexamination
PROTIGAL ET AL.Examiner
A. SeferArt Unit
2826

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-4,656,605	04-1987	Clayton	365/52
	B	US-4,903,113	02-1990	Frankeny et al	357/70
	C	US-3,566,203	02-1971	Maguire et al	317/230
	D	US-4,616,655	10-1986	Weinberg et al	128/419
	E	US-4,695,870	09-1987	Patraw	357/74
	F	US-4,695,678	09-1987	Itagaki et al	174/52
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 61-73367	04-1986	Japan	Matsumoto	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"On-chip decoupling capacitor for logic VLSI chips," page 1280, IBM technical disclosure bulletin, Vol. 30 No. 3, Aug. 1987.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.